

103

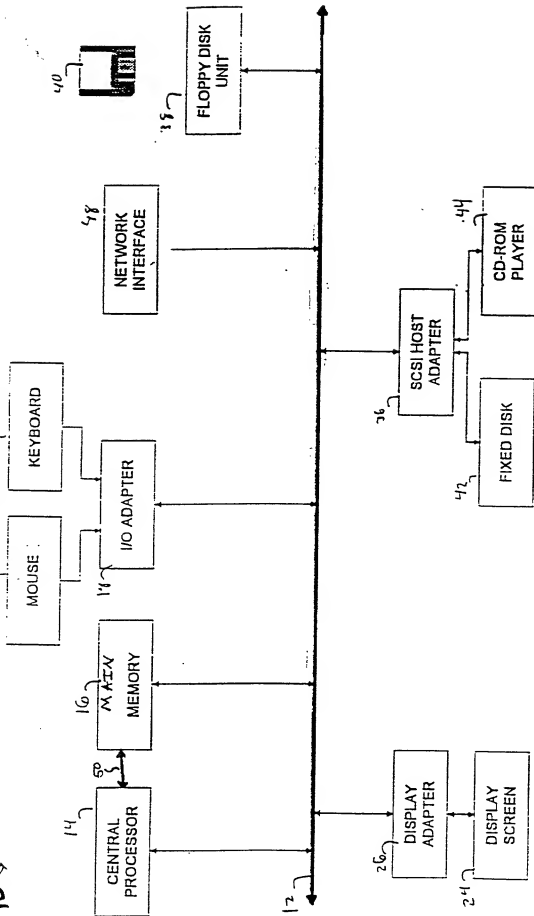


Fig. 1A
(Prior Art)

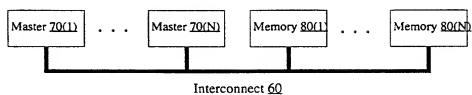


Fig. 1B

(Don't int)

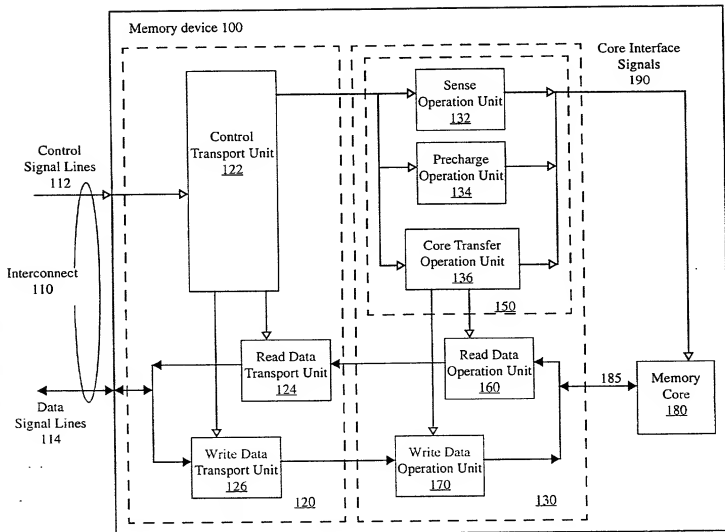


Fig. 1C

(Prior Art)

10014457-1-1100

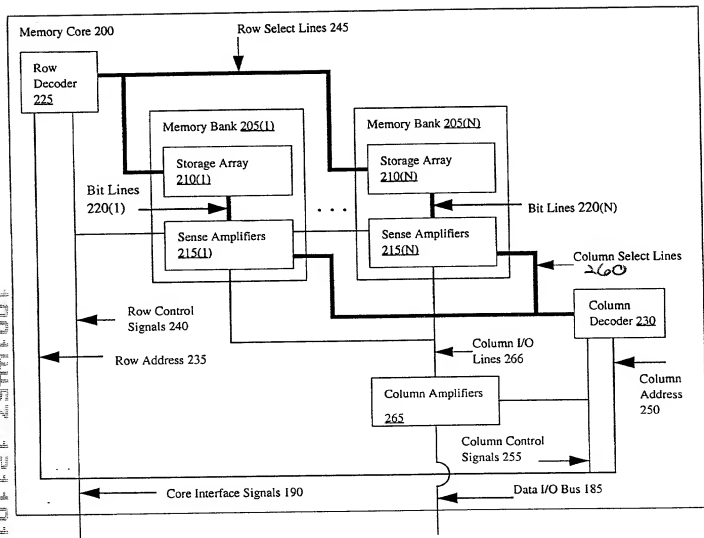


Fig. 2

(Prior Art)

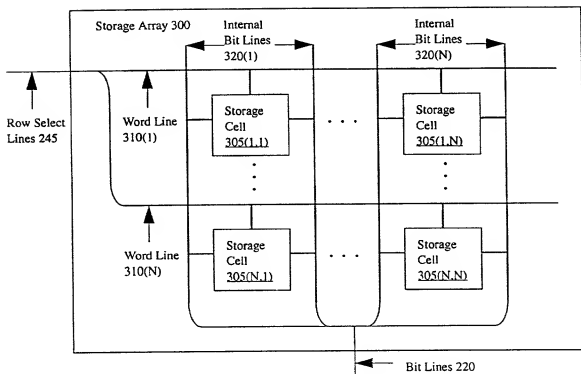


Fig. 3
(Prior Art)

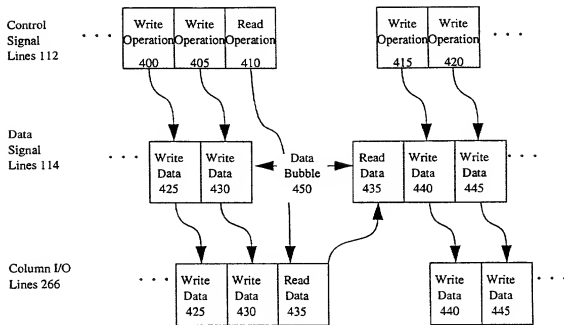


Fig. 4

(Prior art)

Control
Signal
Lines 112

Data
Signal
Lines 114

Column I/O Lines 266
(Device A)

Column I/O Lines 266
(Device B)

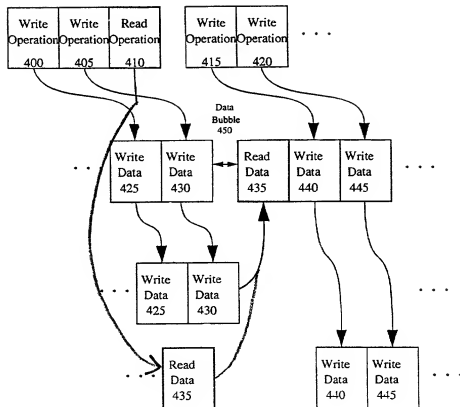


Fig. 5

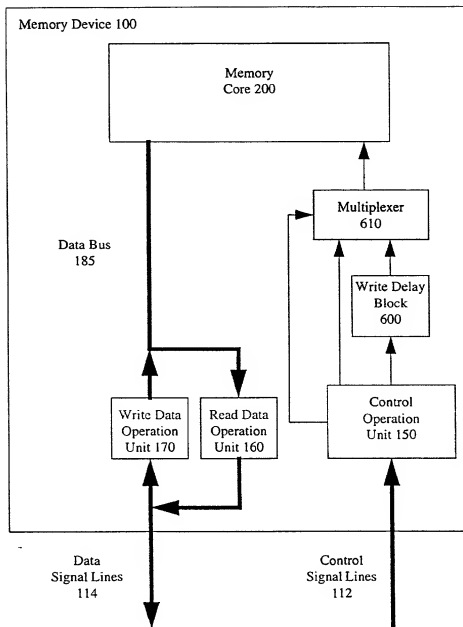


Fig. 6

1004457-121101

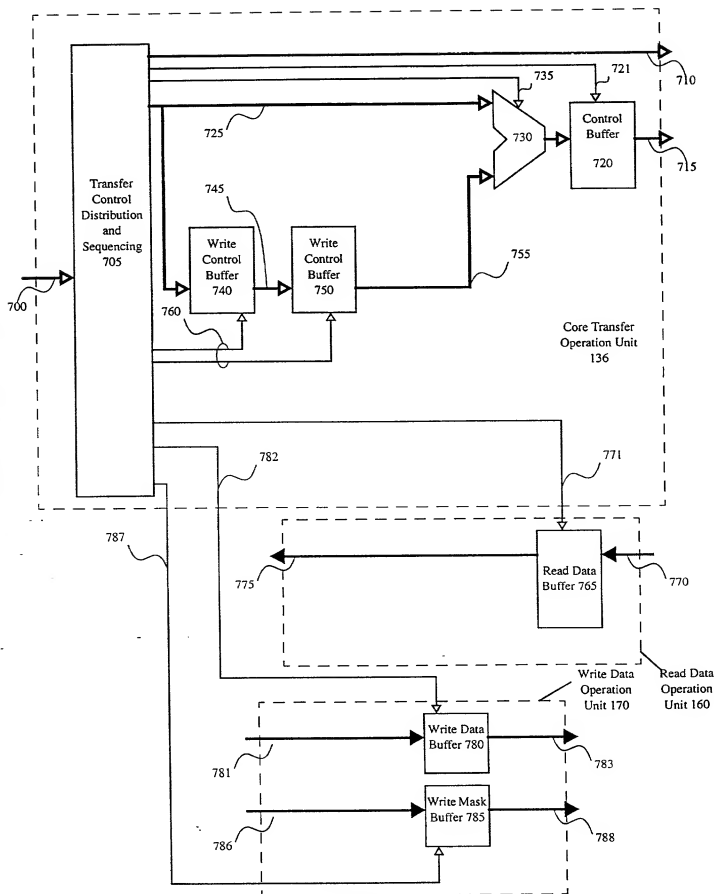


Fig. 7

Control Signal
Lines 112

Data Signal
Lines 114

Column I/O
710&
715

Read Data Buffer
775Write Data Buffer
783

Write Mask Buffer
788 ' '

Write Control Buffer
755

Write Control Buffer
745

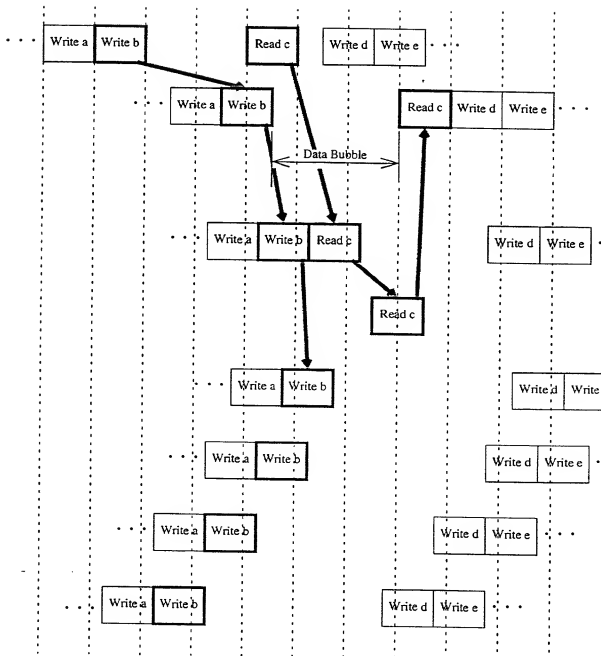


Fig. 8

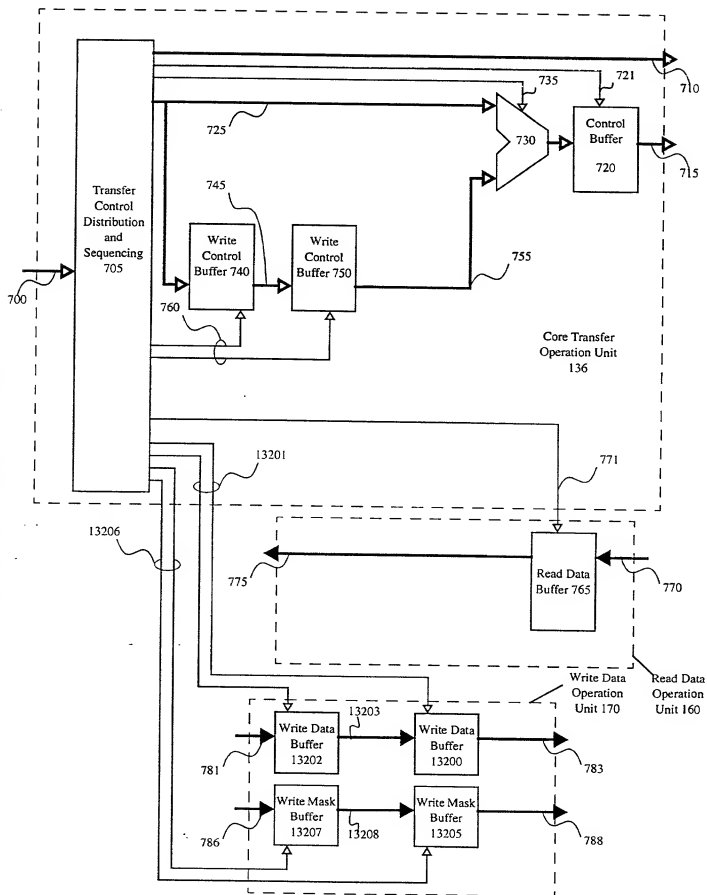


Fig. 9

10014457-321101

Control Signal
Lines 112

Data Signal
Lines 114

Column I/O
710&
715

Read Data Buffer
775

Write Data Buffer
783

Write Data Buffer
13203

Write Mask Buffer
789

Write Mask Buffer
13208

Write Control Buffer
755

Write Control Buffer
745

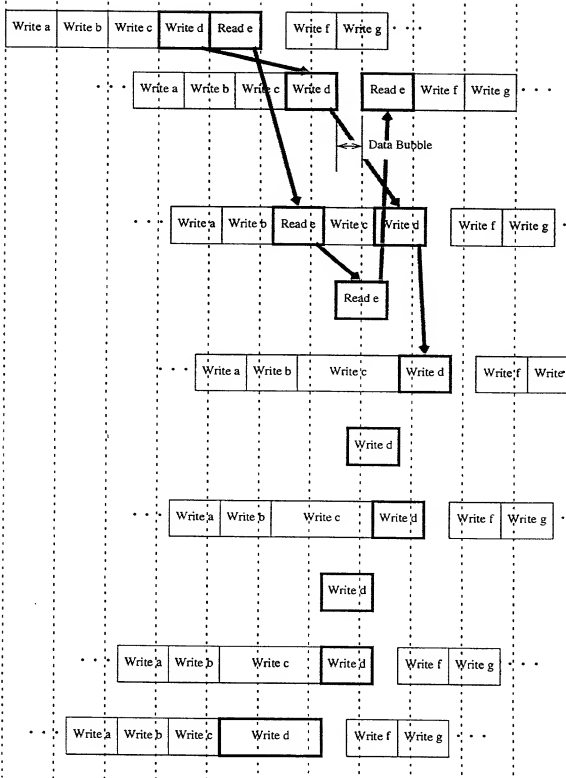


Fig. 10

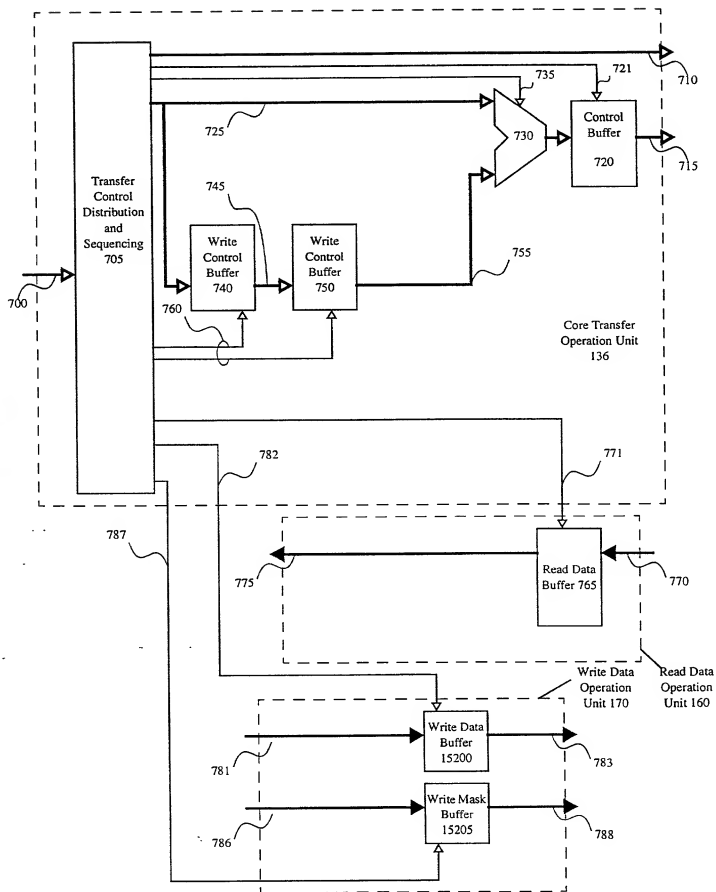


Fig. 11

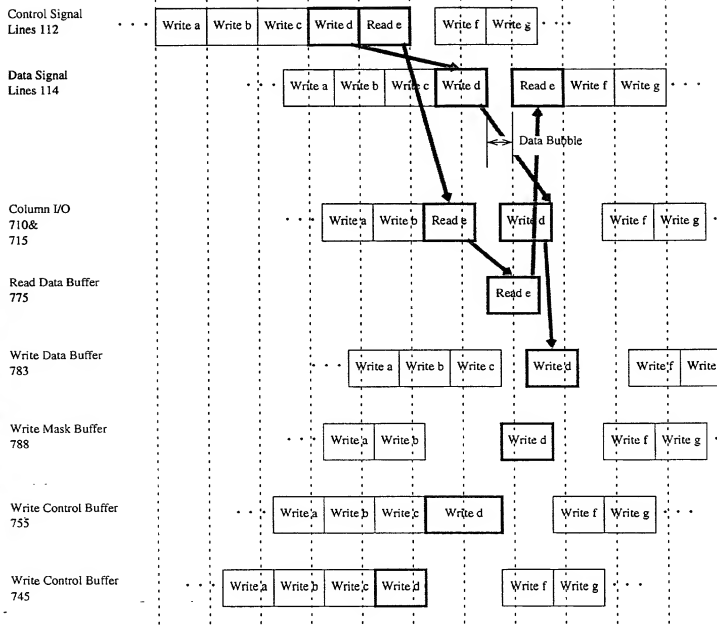


Fig. 12

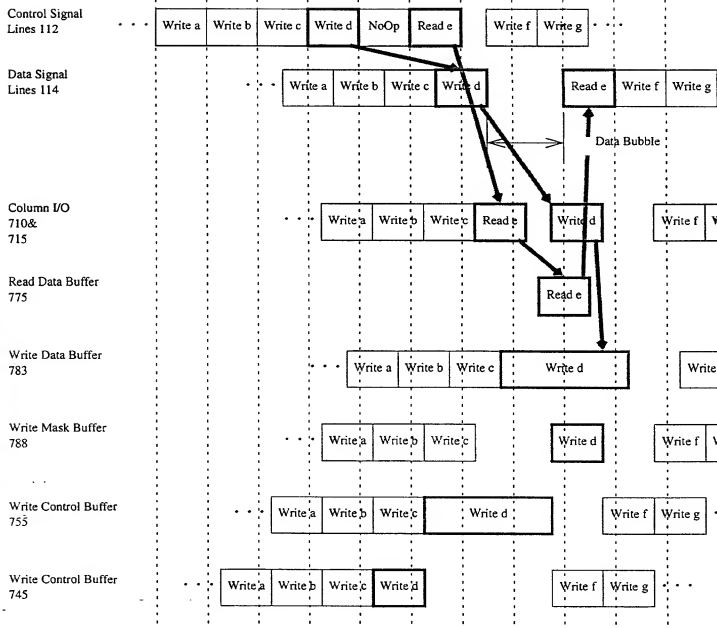


Fig. 13

Control Signal
Lines 112

Data Signal
Lines 114

Column I/O
710&
715

Read Data Buffer
775

Write Data Buffer
783

Write Mask Buffer
788

Write Control Buffer
755

Write Control Buffer
745

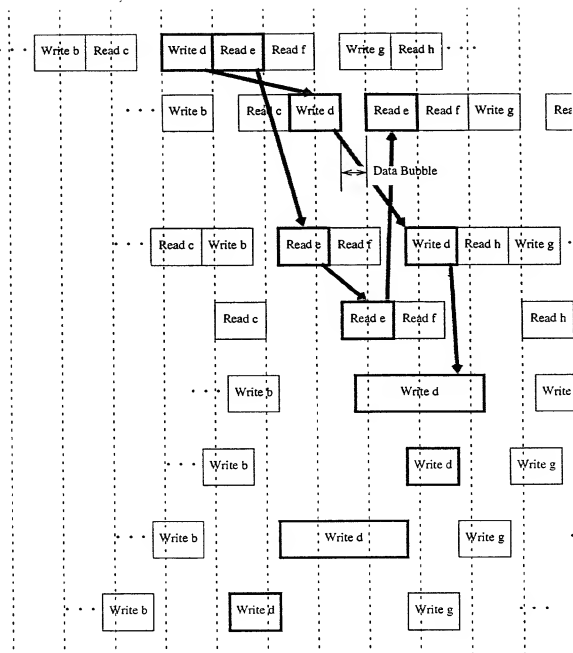


Fig. 14

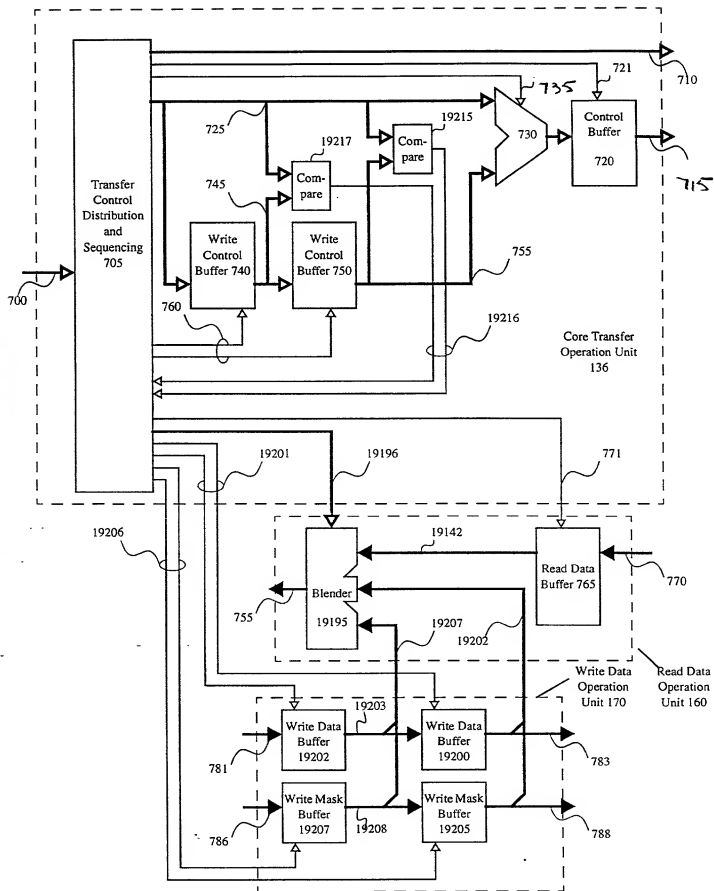


Fig. 15

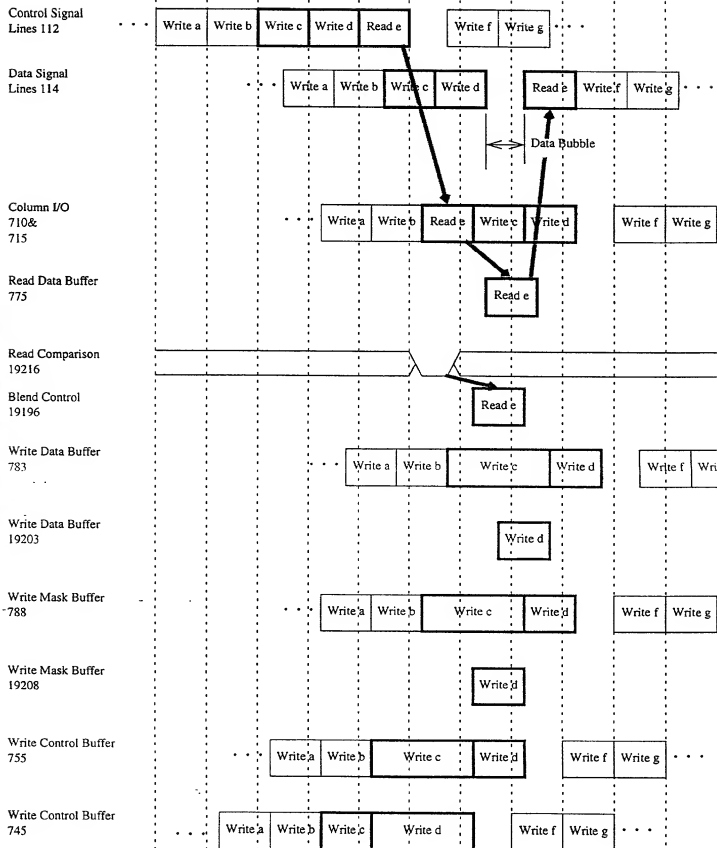


Fig. 17

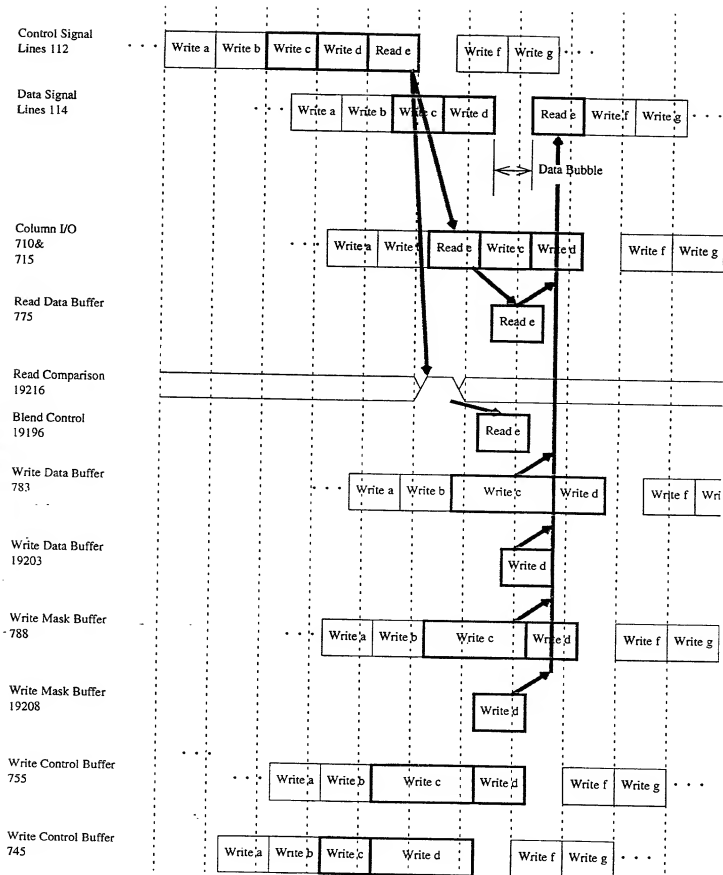


Fig. 18